REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-52 are pending in the application. The Examiner additionally stated that claims 1-52 are rejected. By this amendment, claims 1 and 5 have been amended. Hence, claims 1-52 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to update and correct a mistake in the cross-reference to related applications information. No new matter is presented.

In the Claims

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1-6, 10, 12-15, 18-24, 26-32, 38-43, and 45 under 35 U.S.C. 102(b) as being anticipated by Isaman (6,035,391) (hereinafter, *Isaman*). Applicant respectfully traverses the Examiner's rejections.

With respect to claim 1, the Examiner stated that *Isaman* and a dictionary definition of a branch target buffer disclose a branch target address cache, coupled to a fetch address, for providing offset information relating to a location of a branch instruction within a line of instruction bytes. Applicant respectfully asserts that *Isaman* does not teach a branch target address cache (BTAC), coupled to a fetch address, for predicting a target address of a branch instruction contained in a line of instruction bytes output by an instruction cache selected by the fetch address, and for providing offset information relating to a location of the branch instruction, as recited in amended claim 1. The cited dictionary definition teaches that a BTB stores the predicted destination (or target address) of a branch instruction. The target address of a predicted branch instruction is the address of the target instruction to which the predicted branch instruction will branch. Thus, the target address is related to the location of the target instruction, but has no relation to the address of the predicted branch instruction itself. Thus, neither *Isaman* nor the dictionary definition, alone or in combination, teach a BTAC that provides a predicted target

address of a branch instruction and offset information relating to a location of the branch instruction within a cache line of instruction bytes containing the predicted branch instruction, as recited in claim 1.

The Examiner states when the target line (i.e., the line containing the target instruction) pointed to by the target address contains a branch instruction, the offset or target address relates to a location of the branch instruction within that cache line of instruction bytes. Applicant has amended claim 1 to clarify that the branch instruction to whose location the offset information relates is the branch instruction whose target address is being predicted by the BTAC, rather than to a branch instruction that might be the target instruction. Thus, neither *Isaman* nor the dictionary definition, alone or in combination, teach a BTAC that provides a predicted target address of a branch instruction and offset information relating to a location of the branch instruction within a cache line of instruction bytes containing the predicted branch instruction, as recited in claim 1.

Further with respect to claim 1, the Examiner stated that *Isaman* discloses selection logic, coupled to the BTAC, for causing a portion of the instruction bytes not to be provided to the instruction buffer, based on the offset information. Applicant respectfully asserts that neither *Isaman* nor the dictionary definition, alone or in combination, teach selection logic for causing a portion of the instruction bytes to not be provided to the instruction buffer, based on the offset information, as recited in amended claim 1. The Examiner states that *Isaman*'s instruction parser separates an instruction line into separate instruction buffers based on BTB offset information when the BTB provided the offset or target address for which to fetch the current line of instructions, citing figure 3 and column 8, lines 1-13 of *Isaman*. As explained above, claim 1 has been amended to clarify that the offset information relates to the branch instruction whose target address is being predicted by the BTAC, rather than to a branch instruction that might be the target instruction. Thus, neither *Isaman* nor the dictionary definition, alone or in combination, teach a BTAC that provides a predicted target address of a branch instruction and offset information relating to a location of the branch instruction within a cache line of instruction bytes containing the predicted branch instruction, as recited in claim 1. Furthermore, the cited text and figure of *Isaman* do not teach parsing instructions based

on information provided by *Isaman*'s BTB, and Applicant can find no such teaching in *Isaman*.

For these reasons, Applicant respectfully requests that the Examiner withdraw his rejection to claim 1.

With respect to claims 2-25 and 47-48, these claims depend from claim 1 and add further limitations that are not anticipated by *Isaman*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 2-25 and 47-48.

With respect to claim 26, the Examiner stated the limitations are substantially similar to the limitations given in claims 1-26 and thus the same arguments given for those claims apply as well. Applicant respectfully asserts that *Isaman* does not anticipate claim 26 for the reasons stated above with respect to amended claim 1. In particular, neither *Isaman* nor the dictionary definition, alone or in combination, teach selection logic that writes a branch instruction and a target instruction of the branch instruction immediately adjacent to one another into an instruction buffer, as recited in claim 26.

For these reasons, Applicant respectfully requests that the Examiner withdraw his rejection to claim 26.

With respect to claims 27-37 and 49-50, these claims depend from claim 26 and add further limitations that are not anticipated by *Isaman*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 27-37 and 49-50.

With respect to claim 38, the Examiner stated the limitations are substantially similar to the limitations given in claims 1-26 and thus the same arguments given for those claims apply as well. Applicant respectfully asserts that *Isaman* does not anticipate claim 38 for the reasons stated above with respect to amended claim 1. In particular, neither *Isaman* nor the dictionary definition, alone or in combination, teach providing to an instruction buffer a portion of first and second cache lines remaining after discarding instructions after a branch instruction in the first cache line and after discarding instructions preceding the target instruction of the branch instruction in the second cache line, as recited in claim 38.

For these reasons, Applicant respectfully requests that the Examiner withdraw his rejection to claim 38.

With respect to claims 39-46 and 51-52, these claims depend from claim 38 and add further limitations that are not anticipated by *Isaman*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 39-46 and 51-52.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 1-52 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Finally, Applicant directs the Examiner's attention to an Information Disclosure Statement (IDS) recently submitted on 7/11/05 in relation to the instant application. Applicant requests that the Examiner review the information in detail, independently evaluate each item carefully in the consideration of the pending claims, and return an initialed copy of each form to the undersigned practitioner.

EXPRESS MAIL LABEL NUMBER: EQ 005 259 006 US
DATE OF DEPOSIT: 7/13/05
I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop _____ , Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

_____ /E. Alan Davis/ _____ .

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_____ 7/13/2005 _____ .